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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,791	09/08/2003	Kia Silverbrook	BAL52US	8951

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393 DARLING STREET
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AUSTRALIA

EXAMINER
MENBERU, BENIYAM

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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	Application No.	Applicant(s)
	10/656,791	SILVERBROOK, KIA
Office Action Summary	Examiner	Art Unit	
	BENIYAM MENBERU	2625	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>07 June 2010</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
    closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-3 and 7-11</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-3 and 7-11</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☒ None of:

    1. ☒ Certified copies of the priority documents have been received.

    2. ☐ Certified copies of the priority documents have been received in Application No. _____.

    3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
        application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Response to Arguments

1.   The terminal disclaimer filed on June 7, 2010 disclaiming the terminal portion of

any patent granted on this application which would extend beyond the expiration date of

U.S. Patent No. 7483053 has been reviewed and is accepted. The terminal disclaimer

has been recorded.

2.   **Claims 1-3 and 7-11 are now rejected based on nonstatutory obviousness-**

type double patenting using a new ground of rejection of U.S. Patent No. 6879341

to Silverbrook.

Double Patenting

1.   The nonstatutory double patenting rejection is based on a judicially created
doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the
unjustified or improper timewise extension of the "right to exclude" granted by a patent
and to prevent possible harassment by multiple assignees.   A nonstatutory
obviousness-type double patenting rejection is appropriate where the conflicting claims
are not identical, but at least one examined application claim is not patentably distinct
from the reference claim(s) because the examined application claim is either anticipated
by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140
F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29
USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.
1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422
F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163
USPQ 644 (CCPA 1969).
        A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d)
may be used to overcome an actual or provisional rejection based on a nonstatutory
double patenting ground provided the conflicting application or patent either is shown to

be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2.   Claims 1, 2, and 7 are rejected on the ground of nonstatutory obviousness-type

double patenting as being unpatentable over claims 1 and 4 of U.S. Patent No. 6879341

to Silverbrook in view of XP-002353310, "VLIW Processor Architecture Adapted to

FPAs" to Petit et al further in view of U.S. Patent No. 4975969 to Tal further in view of

U.S. Patent No. 5852502 to Beckett.

        Regarding claim 1, Silverbrook '341 discloses an image sensing and printing

digital camera device (see claim 1, lines 1-3 and lines 17-19; Silverbrook '341)

comprising:

receiving a printed instruction card having printed thereon an array of dots representing

a programming script (see claim 4, lines 1-4 wherein Silverbrook '341 discloses a card

that has "a card carrying a two-dimensional optical code that defines the image

processing instructions" in contrast to printed instruction card as claimed but it is

obvious that the optical code is printed on the card since it is optically scanned;

Silverbrook '341 discloses "two-dimensional optical code" in contrast to the array of dots

as claimed but it is obvious that a two-dimensional optical code can define an array of

dots; Silverbrook '341 discloses wherein the optical code defines a "image processing

instructions" in contrast to a programming script as claimed but it is obvious that

processing instructions can define a program script);

an area image sensor positioned on the housing for sensing a viewed image and for generating pixel data representing the viewed image (see claim 1, lines 2-3; Silverbrook '341 discloses a camera comprising a sensor in contrast to a housing for positioning an image sensor but it is obvious that since the image sensor is in the camera it must be in a housing; Silverbrook '341 discloses sensing an image and generating "signal carrying image data" in contrast to sensing viewed image and pixel data generation as claimed but it is obvious that the image data is image viewed through the camera and it is also obvious that "signal carrying image data" can define pixel data of a viewed image data in a digital camera;);

a linear image sensor for scanning the printed instruction card and converting the array of dots into a data signal (see claim 1, lines 4-5; claim 4, lines 1-4; Silverbrook '341 discloses a reader for optical code in contrast to a linear image sensor as claimed but it is obvious that a reader which reads optical data can be linear image type sensor; Silverbrook '341 discloses a "card carrying a two-dimensional optical code that defines the image processing instructions" in contrast to printed instruction card but it is obvious that the optical code is printed on the card since it is optically scanned; Silverbrook '341 discloses "two-dimensional optical code" in contrast to the array of dots as claimed but it is obvious that a two-dimensional optical code can define an array of dots; Silverbrook '341 discloses wherein the read instructions from the optical code is used to generate "signal carrying processing data" in contrast to converting the array of dots into data signal as claimed but it is obvious that generation of the "signal carrying processing data" from the instruction can define a conversion process);

a printing mechanism arranged on the housing (see claim 1, lines 17-19; Silverbrook

'341 discloses a camera comprising a printer in contrast to a housing that arranges a

printer but it is obvious that since the printer is in the camera it must be in a housing;);

integrating a processor, an area image sensor interface connected to the processor, a

linear image sensor interface, and a printhead interface connected to the processor

(see claim 1, lines 6-14, 17-19; Silverbrook '341 discloses processing units connected to

the "image sensor", "reader", and printer in contrast to the integration of the processor,

area image sensor interface, linear image sensor interface, and printhead interface but

it is obvious that since the processing units, "image sensor", "reader", and printer are in

the camera they are integrated; Silverbrook '341 discloses of processing units

connected to the "image sensor", "reader", and printer in contrast to an area image

sensor interface, linear image sensor interface, and printhead interface as claimed but

is obvious that these connection defines an interface to each of the respective units

wherein the "image sensor" defines area image sensor, "reader" defines the linear

image sensor and printer defines the printhead; Further Silverbrook '341 defines a

"printer connected to the processing units" "for printing the processed image" in contrast

to a printhead interface connected to the processor but it is obvious that a printer

provides a printhead for printing image data),

and receiving the pixel data and the data signal, to effect communication of the pixel

data and the data signal thereto (see claim 1, lines 4-14; Silverbrook '341 discloses the

reception of "image data" and "processing data" in contrast to the

receiving/communication of pixel data and data signal as claimed but it is obvious that

the image data defines the pixel data in a digital camera and the "processing data" can

be data signal and the receiving of data defines communication), wherein decodes the

data signal into the programming script and executes the programming script

represented by the array of dots on the pixel data (see claim 1, lines 6-14; claim 4, lines

1-4; Silverbrook '341 discloses "processing the image data in accordance with the

image processing instructions" wherein the processing instructions are defined from the

optical code in contrast to decoding of data signal and execution of programming script

as claimed but it is obvious that the converting of optical code into processing

instruction defines the decoding and that the instructions define programming scripts

and also the processing of image based on the instructions define the execution of the

programming script; Silverbrook '341 discloses "two-dimensional optical code" in

contrast to the array of dots as claimed but it is obvious that a two-dimensional optical

code can define an array of dots;).

   However Silverbrook '341 does not disclose wherein a VLIW processor is

integrated on a one chip microcontroller provided in the housing.

   Petit et al '310 discloses wherein a VLIW processor is integrated on a one chip

microcontroller provided in the housing (Figure 1, CMOS image sensor; Introduction

second paragraph; Figure 1, shows one-chip microcontroller; see Abstract; Introduction

first paragraph; Figure 1, shows VLIW processor integrated on the one-chip;

Introduction sixth paragraph; The dashed lines in Figure 1 defines the housing for the

one-chip device; Figure 1, shows interface between CMOS sensor and ADC (analog to

digital converter); Introduction seventh paragraph).

Having the system of **Silverbrook '341** and then given the well-established

teaching of **Petit et al '310**, it would have been obvious to one of ordinary skill in the art

at the time of the invention was made to modify the system of **Silverbrook '341** as

taught by **Petit et al '310**, since **Petit et al '310** stated in Abstract and first and fourth

paragraph of the Introduction, such a modification would provide an efficient and

productive processor using a VLIW type processor.

However Silverbrook '341 does not disclose a housing defining a slot for

receiving card.

Tal '969 discloses disclose a housing defining a slot for receiving card (Figure 3,

slot 87; interface for camera 60; and interface for card reader 70; column 7, lines 48-

68).

Having the system of **Silverbrook '341** and then given the well-established

teaching of **Tal '969**, it would have been obvious to one of ordinary skill in the art at the

time of the invention was made to modify the system of **Silverbrook '341** as taught by

Tal '969, since **Tal '969** stated in col. 7, lines 48-55; col. 8, lines 40-56, such a

modification would provide a card reader slot for inputting a card having useful

information stored in it.

However Silverbrook '341 does not disclose wherein the receiving of the pixel

data and data signal is by an input buffer connected to both the area image sensor

interface and the linear image sensor interface and wherein the input buffer being

further connected to the processor.

Beckett '502 discloses wherein the receiving of the pixel data and data signal

(column 6, lines 38-55; the color and monochrome pixel defines the pixel data and data

signal) is by an input buffer connected to both the area image sensor interface and the

linear image sensor interface and wherein the input buffer being further connected to

the processor (Figure 1 shows a frame buffer 38 (input buffer) which is connected to a

color sensor 24 and a monochrome sensor 22; column 4, lines 10-16, 36-42; connecting

lines 36 and 34 defines the interface for the color sensor 24 and monochrome sensor

22 respectively. Further buffer 38 is connected to a processor 44; column 5, lines 17-24;

column 7, lines 17-22; column 8, lines 17-22; Further the processor 44 can be defined in

terms of a CPU. column 5, lines 44-56; since the color sensor and monochrome sensor

are two-dimensional arrays of pixel they both can be defined as an area sensor and a

linear sensor. So either of the color sensor 24 or monochrome sensor 22 can be a area

image sensor or linear image sensor.).

Having the system of *Silverbrook '341* and then given the well-established

teaching of *Beckett '502*, it would have been obvious to one of ordinary skill in the art at

the time of the invention was made to modify the system of *Silverbrook '341* as taught

by *Beckett '502*, since *Beckett '502* stated in col. 4, lines 50-64; col. 7, lines 11-16,

such a modification would provide a temporary holding place for image data before

processing.

Regarding claim 2, Further Beckett '502 discloses a device as claimed in claim 1, wherein the area image sensor is one of a charge coupled device and an active pixel sensor (column 4, lines 10-15).

Regarding claim 7, Further Silverbrook '341 discloses a device as claimed in claim 1, wherein the array of dots is a two-dimensional array (see claim 4; "two dimensional optical code") and wherein the linear image sensor is an optical reader (see Beckett '502: column 4, lines 8, 10-15; column 5, lines 45-48).

3.   Claims 3, 8, and 10 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 4 of U.S. Patent No. 6879341 to Silverbrook in view of XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al further in view of U.S. Patent No. 4975969 to Tal further in view of U.S. Patent No. 5852502 to Beckett further in view of U.S. Patent No. 5875034 to Shintani et al.

Regarding claim 3, claims 1 and 4 of U.S. Patent No. 6879341 to Silverbrook in view of Petit et al '310 further in view of Tal '699 further in view of Beckett '502 does not disclose a device as claimed in claim 1, wherein the printing mechanism includes an ink distribution assembly that is mounted on the print head assembly to distribute ink to the print head chips.

Shintani et al '034 discloses a device as claimed in claim 1, wherein the printing mechanism includes an ink distribution assembly that is mounted on the print

head assembly to distribute ink to the print head chips (column 18, lines 1-9, head 410
is pressed onto ink ribbon).

Having the system of **Silverbrook '341 in view of Petit et al '310 further in
view of Tal '969 further in view of Beckett '502** and then given the well-established
teaching of **Shintani et al '034**, it would have been obvious to one of ordinary skill in the
art at the time of the invention was made to modify the system of **Silverbrook '341 in
view of Petit et al '310 further in view of Tal '969 further in view of Beckett '502** as
taught by **Shintani et al '034**, since **Shintani et al '034** stated in col. 3, Lines 55-67;
column 4, lines 1-2, such a modification would provide a camera with embedded printer
for providing user specified mode of printing.

Regarding claim 8, Further Petit et al '310 discloses the device as claimed in
Claim 7, wherein the one-chip microcontroller includes a program memory (Figure 1, the
one-chip has **<u>instruction (program)</u>** and data memory), and the one-chip
microcontroller is operable to write the program script to the program memory (page
129, fourth paragraph; instructions are stored in instruction memory) and Shintani et al
'034 discloses further operable to run the program script from the program memory to
define a software algorithm by which registers in the printhead interface are addressed
to apply a desired effect to the pixel data (processor 100 is programmed to execute
processing (column 13, lines 16-20); Figure 1, processor 100 interfaces the printing
section 111; column 13, lines 1-15; "desired print system" on column 13, line 11; column
13, lines 16-20, 56-61; One desired effect is multi-image effect which can print multi-
image. Column 19, lines 9-25; head unit contains registers 501, 502).

Regarding claim 10, Further Petit et al '310 discloses the device as claimed in claim 8, wherein the VLIW processor receives pixel data from the image sensor, converts the pixel data into an internal format, and writes the converted pixel data to the DRAM memory interface (Introduction: seventh and eighth paragraph; ADC converts to digital format for writing into register; Figure 1 shows data memory control unit which interfaces with SLDRAM; page 131 paragraph before "SIMULATION RESULTS" section.).

4.   Claims 9 and 11 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 4 of U.S. Patent No. 6879341 to Silverbrook in view of XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al further in view of U.S. Patent No. 4975969 to Tal further in view of U.S. Patent No. 5852502 to Beckett further in view of U.S. Patent No. 6094282 to Hoda et al.

Regarding claim 9, Petit et al '310 discloses a one-chip microcontroller and a VLIW processor (Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph; Figure 1, shows VLIW processor integrated on the one-chip; Introduction sixth paragraph). However claims 1 and 4 of U.S. Patent No. 6879341 to Silverbrook in view of Petit et al '310 further in view of Tal '699 further in view of Beckett '502 does not disclose the device as claimed in claim 1, further including an output

buffer, the output buffer effecting communication between the processor and the
printhead interface.

Hoda et al '282 discloses an output buffer, the output buffer effecting
communication between the processor and the printhead interface (Figure 5 shows
processor 415 in communication with memory 418 (output buffer) which is connected to
printhead unit 419; column 8, lines 24-42, 61-67).

Having the system of *Silverbrook '341 in view of Petit et al '310 further in
view of Tal '969 further in view of Beckett '502* and then given the well-established
teaching of *Hoda et al '282*, it would have been obvious to one of ordinary skill in the art
at the time of the invention was made to modify the system of *Silverbrook '341 in view
of Petit et al '310 further in view of Tal '969 further in view of Beckett '502* as taught
by *Hoda et al '282*, since *Hoda et al '282* stated in col. 8, lines 37-42, 61-67, such a
modification would provide the buffering of a line of printing data for the printhead
system.

Regarding claim 11, Petit et al '310 discloses the VLIW processor (Figure 1,
shows VLIW processor integrated on the one-chip; Introduction sixth paragraph).
Further Hoda et al '282 discloses the device as claimed in claim 9, wherein the
processor converts the pixel data to print image data, and writes the print image data to
the output buffer (column 8, lines 20-34, 37-42; processor converts image data to print
data using data from Table 417. the converted data is output to memory 418 (output
buffer).).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENIYAM MENBERU whose telephone number is (571) 272-7465. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on (571) 272-7437. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is (571) 272-2600. The group receptionist number for TC 2600 is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patent Examiner
Beniyam Menberu

/Beniyam Menberu/
Examiner, Art Unit 2625

08/11/2010

/David K Moore/

Supervisory Patent Examiner, Art Unit 2625